IN THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the Application:

LISTING OF CLAIMS:

Claims 1-2 (Canceled).

3. (Currently Amended) ~~The data storage system of claim 2 wherein the packaged microcontroller further includes:~~ A data storage system, comprising:

power circuitry configured to provide power signals;

storage processing circuitry configured to perform data storage operations; and

a packaged microcontroller coupled to the power circuitry and the storage processing circuitry, the packaged microcontroller having a set of input lines, a set of output lines, and control circuitry coupled to the set of input lines and the set of output lines, the control circuitry being configured to:

receive, on the set of input lines, a first set of power signals which is provided by the power circuitry to the storage processing circuitry,

wait a predetermined time period in response to receipt of the first set of power signals on the set of input lines, and

output, through the set of output lines, a set of enable signals to the power circuitry after waiting the predetermined time period, the set of enable signals directing the power circuitry to provide a second set of power signals to the storage processing circuitry;

wherein the packaged microcontroller further includes:

a set of built-in analog-to-digital converters coupled to the set of input lines and to the control circuitry, the control circuitry being configured to compare a set of binary values from the set of built-in analog-to-digital converters to a set of pre-determined thresholds to determine when all of the power signals within the set of power signals have reached levels that

prevents damage to the storage processing circuitry when the second set of power signals is provided to the storage processing circuitry;

memory which stores pre-loaded code having a version identifier, the control circuitry being configured to:

compare the version identifier of the pre-loaded code with a version identifier of available new code, and

replace the pre-loaded code stored in the memory with the available new code when the version identifier of the available new code indicates that the available new code is newer than the pre-loaded code, and maintain the pre-loaded code within the memory when the version identifier of the available new code indicates that the available new code is not newer than the pre-loaded code.

4. (Original) The data storage system of claim 3 wherein the packaged microcontroller further includes:

a dedicated memory location, wherein the control circuitry, when replacing the pre-loaded code stored in the memory with the available new code, is configured to:

set the dedicated memory location with a flag to indicate that a code replacement routine is in progress,

overwrite the pre-loaded code stored in the memory with the available new code, and

clear the dedicated memory location to remove the flag to indicate that no code replacement routine is in progress.

5. (Currently Amended) The data storage system of claim ~~2~~ 3, further comprising:

a power button,

wherein the packaged microcontroller further includes a dedicated ~~persistent~~ memory location, the control circuitry being configured to:

access the dedicated ~~persistent~~ memory location to determine whether the power button of has been toggled to an "ON" position or an "OFF" position, and

place the storage processing circuitry in one of (i) a normal operating state when the dedicated ~~persistent~~ memory location indicates that the power button has been toggled to the "ON" position, and (ii) a recovery state when the dedicated ~~persistent~~ memory location indicates that the power button has been toggled to the "OFF" position.

Claims 6-7 (Canceled).

8. (Currently Amended) ~~The packaged microcontroller of claim 7, further comprising:~~ A packaged microcontroller for controlling a data storage system having (i) power circuitry for providing power signals and (ii) storage processing circuitry for performing data storage operations, the packaged microcontroller comprising:

a set of input lines;

a set of output lines;

control circuitry coupled to the set of input lines and the set of output lines, the control circuitry being configured to:

receive, on the set of input lines, a first set of power signals which is provided by the power circuitry to the storage processing circuitry,

wait a predetermined time period in response to receipt of the first set of power signals on the set of input lines; and

output, through the set of output lines, a set of enable signals to the power circuitry after waiting the predetermined time period, the set of enable signals directing the power circuitry to provide a second set of power signals to the storage processing circuitry;

a set of built-in analog-to-digital converters coupled to the set of input lines and to the control circuitry, the control circuitry being configured to compare a set of binary values from the set of built-in analog-to-digital converters to a set of

pre-determined thresholds to determine when all of the power signals within the set of power signals have reached levels that prevents damage to the storage processing circuitry when the second set of power signals is provided to the storage processing circuitry; and

memory which stores pre-loaded code having a version identifier, the control circuitry being configured to:

compare the version identifier of the pre-loaded code with a version identifier of available new code; and

replace the pre-loaded code stored in the memory with the available new code when the version identifier of the available new code indicates that the available new code is newer than the pre-loaded code, and maintain the pre-loaded code within the memory when the version identifier of the available new code indicates that the available new code is not newer than the pre-loaded code.

9. (Original) The packaged microcontroller of claim 8, further comprising:

a dedicated memory location, wherein the control circuitry, when replacing the pre-loaded code stored in the memory with the available new code, is configured to:

set the dedicated memory location with a flag to indicate that a code replacement routine is in progress,

overwrite the pre-loaded code stored in the memory with the available new code, and

clear the dedicated memory location to remove the flag to indicate that no code replacement routine is in progress.

10. (Currently Amended) ~~The packaged microcontroller of claim 7, further comprising:~~ A packaged microcontroller for controlling a data storage system having (i) power circuitry for providing power signals and (ii) storage processing circuitry for performing data storage operations, the packaged microcontroller comprising:

a set of input lines;

a set of output lines;

control circuitry coupled to the set of input lines and the set of output lines, the control circuitry being configured to:

receive, on the set of input lines, a first set of power signals which is provided by the power circuitry to the storage processing circuitry,

wait a predetermined time period in response to receipt of the first set of power signals on the set of input lines; and

output, through the set of output lines, a set of enable signals to the power circuitry after waiting the predetermined time period, the set of enable signals directing the power circuitry to provide a second set of power signals to the storage processing circuitry;

a set of built-in analog-to-digital converters coupled to the set of input lines and to the control circuitry, the control circuitry being configured to compare a set of binary values from the set of built-in analog-to-digital converters to a set of pre-determined thresholds to determine when all of the power signals within the set of power signals have reached levels that prevents damage to the storage processing circuitry when the second set of power signals is provided to the storage processing circuitry;

a dedicated memory location; and

memory having a main portion which stores pre-loaded main code and a secondary portion which stores pre-loaded secondary code, wherein the control circuitry is further configured to:

access the dedicated memory location to determine whether a flag is set to indicated that a code replacement routine is in progress, and

run (i) the pre-loaded main code stored in the main portion of the memory when the dedicated memory location is not set with the flag, and (ii) the secondary code stored in the secondary portion of the memory when the dedicated memory location is set with the flag.

11. (Currently Amended) The packaged microcontroller of claim ~~7~~ 8 wherein the data storage system has a power button, and wherein the packaged microcontroller further comprises:

a ~~persistent~~ dedicated memory location, the control circuitry being configured to:

access the dedicated ~~persistent~~ memory location to determine whether the power button of has been toggled to an "ON" position or an "OFF" position, and

place the storage processing circuitry in one of (i) a normal operating state when the dedicated ~~persistent~~ memory location indicates that the power button has been toggled to the "ON" position, and (ii) a recovery state when the dedicated ~~persistent~~ memory location indicates that the power button has been toggled to the "OFF" position.

12. (Original) The packaged microcontroller of claim 11 wherein the control circuitry is further configured to:

prior to placing the storage processing circuit in one of the normal operating state and the recovery state, communicate with another packaged microcontroller to determine whether other storage processing circuitry of the data storage system is entering a normal operating state or a recovery state.

Claims 13-15 (Canceled).

16. (Currently Amended) ~~The method of claim 15~~ In a packaged microcontroller, a method for controlling a data storage system having (i) power circuitry for providing power signals and (ii) storage processing circuitry for performing data storage operations, the method comprising:

receiving, on a set of input lines of the packaged microcontroller, a first set of power signals which is provided by the power circuitry to the storage processing circuitry;

waiting a predetermined time period in response to receipt of the first set of power signals on the set of input lines; and

outputting, on a set of output lines of the packaged microcontroller, a set of enable signals to the power circuitry after waiting the predetermined time period, the set of enable signals directing the power circuitry to provide a second set of power signals to the storage processing circuitry;

wherein the packaged microcontroller includes:

a set of built-in analog-to-digital converters coupled to the set of input lines, and wherein receiving the first set of power signals includes:

comparing a set of binary values from the set of built-in analog-to-digital converters to a set of pre-determined thresholds to determine when all of the power signals within the set of power signals have reached levels that prevents damage to the storage processing circuitry when the second set of power signals is provided to the storage processing circuitry; and

memory which stores pre-loaded code having a version identifier, and wherein the method further comprises:

comparing the version identifier of the pre-loaded code with a version identifier of available new code; and

replacing the pre-loaded code stored in the memory with the available new code when the version identifier of the available new code indicates that the available new code is newer than the pre-loaded code, and maintaining the pre-loaded code within the memory when the version identifier of the available new code indicates that the available new code is not newer than the pre-loaded code.

17. (Original) The method of claim 16 wherein replacing the pre-loaded code stored in the memory with the available new code includes:

setting a dedicated memory location with a flag to indicate that a code replacement routine is in progress;

overwriting the pre-loaded code stored in the memory with the available new code; and

clearing the dedicated memory location to remove the flag to indicate that no code replacement routine is in progress.

18. (Currently Amended) ~~The method of claim 15~~ In a packaged microcontroller, a method for controlling a data storage system having (i) power circuitry for providing power signals and (ii) storage processing circuitry for performing data storage operations, the method comprising:

receiving, on a set of input lines of the packaged microcontroller, a first set of power signals which is provided by the power circuitry to the storage processing circuitry;

waiting a predetermined time period in response to receipt of the first set of power signals on the set of input lines; and

outputting, on a set of output lines of the packaged microcontroller, a set of enable signals to the power circuitry after waiting the predetermined time period, the set of enable signals directing the power circuitry to provide a second set of power signals to the storage processing circuitry;

wherein the packaged microcontroller includes:

a set of built-in analog-to-digital converters coupled to the set of input lines, and wherein receiving the first set of power signals includes:

comparing a set of binary values from the set of built-in analog-to-digital converters to a set of pre-determined thresholds to determine when all of the power signals within the set of power signals have reached levels that prevents damage to the storage processing circuitry when the second set of power signals is provided to the storage processing circuitry; and

memory having a main portion which stores pre-loaded main code and a secondary portion which stores pre-loaded secondary code, and wherein the method further comprises:

accessing a dedicated memory location to determine whether a flag is set to indicated that a code replacement routine is in progress; and

running (i) the pre-loaded main code stored in the main portion of the memory when the dedicated memory location is not set with the flag, and (ii) the secondary code stored in the secondary portion of the memory when the dedicated memory location is set with the flag.

19. (Currently Amended) The method of claim ~~15~~ 16 wherein the data storage system has a power button, and wherein the method further comprises:

accessing a ~~persistent~~ dedicated memory location to determine whether the power button of has been toggled to an "ON" position or an "OFF" position; and

placing the storage processing circuitry in one of (i) a normal operating state when the dedicated ~~persistent~~ memory location indicates that the power button has been toggled to the "ON" position, and (ii) a recovery state when the dedicated ~~persistent~~ memory location indicates that the power button has been toggled to the "OFF" position.

20. (Original) The method of claim 19, further comprises:

prior to placing the storage processing circuit in one of the normal operating state and the recovery state, communicating with another packaged microcontroller to determine whether other storage processing circuitry of the data storage system is entering a normal operating state or a recovery state.

21. (Currently Amended) A data storage system as in claim ~~1~~ 3 wherein the power circuitry includes a variety of power sources, each power source being configured to provide a power signal, which is at a distinct voltage from other power signals provided by other power sources, to an input line of a storage processing circuit of the storage processing circuitry and to an input line of the

packaged microcontroller which is separate from the input line of the storage processing circuit.

22. (Previously Presented) A data storage system as in claim 21 wherein the control circuitry is configured to:

receive, on the set of input lines, a first set of power signals which is provided by the power circuitry to I/O buffer circuitry of the storage processing circuitry;

wait a predetermined time period in response to receipt of the first set of power signals on the set of input lines; and

output, through the set of output lines, a set of enable signals to the power circuitry after waiting the predetermined time period, the set of enable signals directing the power circuitry to provide a second set of power signals, the second set of power signals to power core circuitry of the storage processing circuitry.

23. (Previously Presented) A data storage system as in claim 22 wherein the packaged microcontroller coupled to the power circuitry and the storage processing circuitry, the packaged microcontroller having a set of input lines, a set of output lines, and control circuitry coupled to the set of input lines and the set of output lines is a PIC-type microcontroller.

24. (Currently Amended) A packaged microcontroller as in claim ~~6~~ 8 wherein the control circuitry is configured to:

receive, on the set of input lines, a first set of power signals which is provided by the power circuitry to I/O buffer circuitry of the storage processing circuitry;

wait a predetermined time period in response to receipt of the first set of power signals on the set of input lines; and

output, through the set of output lines, a set of enable signals to the power circuitry after waiting the predetermined time period, the set of enable signals

directing the power circuitry to provide a second set of power signals, the second set of power signals to power core circuitry of the storage processing circuitry.

25. (Previously Presented) A packaged microcontroller as in claim 6 wherein the packaged microcontroller coupled to the power circuitry and the storage processing circuitry, the packaged microcontroller having a set of input lines, a set of output lines, and control circuitry coupled to the set of input lines and the set of output lines is a PIC-type microcontroller.

26. (New) The method of claim 16 wherein:

receiving includes receiving, on the set of input lines, a first set of power signals which is provided by the power circuitry to I/O buffer circuitry of the storage processing circuitry; and

outputting includes outputting , through the set of output lines, a set of enable signals to the power circuitry after waiting the predetermined time period, the set of enable signals directing the power circuitry to provide a second set of power signals, the second set of power signals to power core circuitry of the storage processing circuitry.